

Application No.: 10/054,241
Response dated October 16, 2003
Reply to Office Action of June 18, 2003

REMARKS/ARGUMENTS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

Claims 11-14 stand rejected under 35 USC 102 as being anticipated by Martin et al, U. S. Patent no. 5,214,768.

In the rejection, the Examiner states that the "memory" is the drive subsystem 44. However, referring to FIG. 2B section 33 includes drive subsystems 48. It is not understood how these drive subsystems are memories.

Claims 11-20 also point out that there is an interface state data bus section:

for carrying interface state data, such interface state data bus section being in communication with both:

- (a) the at least one front-end one and the at least one rear-end one of the directors; and
- (b) the memory.

Such an arrangement is not described in Martin et al.

Claims 21-47 point out that there is a plurality of end-user data busses, for carrying end-user data, each one of the plurality of end-user data **busses having a first end coupled to a corresponding one of the plurality of directors and a second end coupled to the memory.**

Such an arrangement is not described in Martin et al.

New claim 48 points out that each one of the directors has an end user data port and an interface state data port, that a cache memory is coupled to the end user data ports of the plurality of directors; and that the directors control end user data transfer with end user data in such end user data transfer passing through the cache memory in response to interface state data passing through the interface state data ports of the directors.

New claim 49 points out that each one of the first directors has an end user data port and an interface state data port, that each one of the second directors having an end user data port and an interface state data port; that a cache memory is coupled to the end user data ports

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of the plurality of first directors and second directors and that the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the cache memory in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.

New claim 50 points out that each one of the directors having a n end user data port and an interface state data port and that the directors control end user data transfer with end user data in such end user data transfer passing to the cache memory through the end user data ports in response to interface state data passing through the interface state data ports of the directors.

New claim 51 points out that each one of the first directors having an end user data port and an interface state data port, each one of the second directors having an end user data port and an interface state data port; and that the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the end user data ports in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.

New claim 52 points out that the directors control end user data transfer with end user data in such data transfer passing to the cache memory through an end user data communication channel in response to interface state data passing through the directors through a different, interface state data communication channel.

New claim 53 points out that the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through an end user communication channel in response to interface

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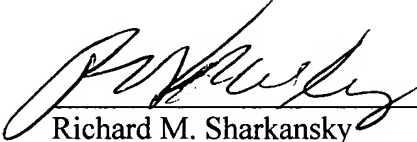
state data passing between the first director and the second director through a different, interface state data communication path.

The remaining new claims also include these limitations referred to above with reference to new claims 48-53 and in addition point out that there is a crossbar switch arranged as claimed.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

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Date


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